

Appl. No. 10/709,428  
Amdt. dated April 28, 2006  
Reply to Office action of March 27, 2006

**REMARKS/ARGUMENTS**

I. Rejection of claims 11, 19, and 33-34 under 35 U.S.C. 102(e):

Claims 11, 19, and 33-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Hatauchi (US 6,858,920).

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**Response:**

The applicant would like to point out how pending claims 11, 19, and 33-34 are patentable over Hatauchi.

10        Claims 11 and 19 each contain limitations stating that "each bonding pad of the chip having a corresponding first lead frame" and the "voltage level of the first lead frames is the logical opposite of the voltage level of the package substrate". In addition claims 11 and 19 also recite that "each bonding pad is selectively connected to the package substrate or the corresponding first lead frame".

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      In this way, each bonding pad can be connected to one of two opposite voltage levels. It should be emphasized that the applicant is not merely claiming that out of a group of bonding pads, some bonding pads are connected to the package substrate and some other bonding pads are connected to a corresponding first lead frame. On the contrary, claims 20 11 and 19 recite that each bonding pad has a corresponding first lead frame, and that the bonding pad is connected to either the package substrate or the corresponding first lead frame.

      On the other hand, Hatauchi fails to teach three limitations of claims 11 and 19. First, 25 Hatauchi does not teach that each bonding pad of the chip has a corresponding first lead frame. As shown in Figure 1 and Figure 2 of Hatauchi, only bonding pads 4a and 4d have a corresponding first lead frame 5. Bonding pads 4b and 4c do not each have their own

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corresponding first lead frame. Second, Hatauchi's disclosure does not teach or suggest that the voltage level of the first lead frame 5 is the logical opposite of the voltage level of the substrate. Third, Hatauchi does not teach that each bonding pad is selectively connected to the package substrate or the corresponding first lead frame. In fact, Hatauchi  
5 does not show the connection of any of the bonding pads 4 to the package substrate.

For these reasons, the applicant submits that claims 11 and 19 are patentably distinguished from Hatauchi, and should therefore be allowable.

10 Regarding claims 33 and 34, each of these claims recites the limitation of "each bonding pad of the chip having a corresponding second lead frame". Furthermore, these claims also recite that "each bonding pad is selectively connected to the package substrate, the corresponding first lead frame, or the corresponding second lead frame".

15 In contrast, Hatauchi does not teach that each bonding pad of the chip has a corresponding second lead frame. As shown in Fig.2 of Hatauchi, each bonding pad 4a only has a corresponding first lead frame 5 (the horizontal lead frames), but no corresponding second lead frame. Similarly, each bonding pad 4d only has a corresponding second lead frame 5 (the vertical lead frames), but no corresponding first  
20 lead frame. Furthermore, bonding pads 4b and 4c do not have corresponding first or second lead frames. Therefore, Hatauchi does not teach the claimed limitations of each bonding pad of the chip having a corresponding first lead frame and a corresponding second lead frame. Because of this, Hatauchi also does not teach the claimed limitation of "each bonding pad is selectively connected to the package substrate, the corresponding  
25 first lead frame, or the corresponding second lead frame".

For the reasons described above, claims 33 and 34 are patentable over Hatauchi, and should be allowed. In addition, claims 33 and 34 are dependent on claims 11 and 19, and

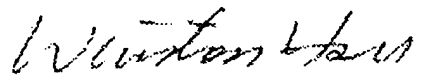
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should be allowed if their respective independent claims are allowed. Reconsideration of claims 11, 19, 33, and 34 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,



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Winston Hsu, Patent Agent No. 41,526

10 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

15 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)